In re Patent Application of:
ROCHE ET AL.
Serial No. **10/039,765**
Filing Date: **NOVEMBER 7, 2001**

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<u>**REMARKS**</u>

Applicants would like to thank the Examiner for the thorough examination of the present application. The claims have been amended to remove the "means language" therefrom. The arguments supporting patentability of the claims are provided below.

I.   The Claimed Invention

The present invention, as recited in independent Claim 20, for example, is directed to a method of transmitting data between two devices via a clock line and at least one data line, with the clock line being maintained by default on a first logic value. The method comprises providing each device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value. The clock line is tied to the second logic value, via the two devices, after data is applied to the data line. The tie to the clock line is maintained by the device to which the data is sent while the device has not read the data. The method further comprises maintaining the data on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent.

The present invention may advantageously provide a double control of the line by which each device – a master or a slave – can be considered as a master as far as the duration of the clock period is concerned. This advantageously allows each device to impose its operating speed on the other, particularly

in the event of disparity of clock frequencies or when one of the devices operates in multitasking on applications that have priority over the data transmission itself.

Independent Claim 32 is similar to independent Claim 20 and is also directed to a method of transmitting data between two devices connected via a clock line and at least one data line.

Independent Claim 44 is similar to independent Claim 20 and is directed to a data transmitting/receiving device.

Independent Claim 46 is similar to independent Claim 20 and is also directed to a data transmitting/receiving device.

Independent Claim 48 is similar to independent Claim 20 and is directed to a synchronous data transmission system.

Independent Claim 51 is similar to independent Claim 20 and is also directed to a communication interface circuit for connection to a data transmitting/receiving device via a clock line and at least one data line.

II.   The Claims Are Patentable

The Examiner rejected independent Claims 20, 32 and 48 over the SPI Block Guide in view of the System Management Bus (SMBus) Specification. The Examiner also rejected independent Claims 44 and 46 over the SPI Block Guide, and independent Claim 51 over the SMBus Specification. All of the claim rejections will be discussed below.

The Examiner has taken the position that FIG. 4-2 on page 27 in the SPI Block Guide illustrates that the clock line is maintained by default on a first logic value (SCK=1), and that one of the devices has the ability to tie the clock line to a

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potential representing a second logic value opposite the first
logic value (SCK=0 at SCK Edge No. 1). The Examiner also
characterized the SPI Block Guide as disclosing that the clock
line is tied to the second logic value, via the two devices,
after data is applied to the data line (data is applied before
SCK Edge No. 1), and data on the data line is maintained by the
device sending the data at least until an instant when the clock
line is released by the device to which the data is sent (data is
applied until rising edge of clock).

As correctly noted by the Examiner, the SPI Block Guide
fails to disclose that the tie to the clock line is maintained by
the device to which the data is sent while the device has not
read the data. The Examiner cited the SMBus Specification as
disclosing this feature. In particular, the Examiner referenced
FIG. 4-7 on page 22 in section 4.3.3. The Examiner has taken the
position that it would have been obvious to have the device
receiving data to hold the clock down, as disclosed by the SMBus
Specification, in the method disclosed by the SPI Block Guide
since this would allow clock synchronization so that slower slave
devices could interface with faster masters.

The Applicants submit that even if the references were
selectively combined as suggested by the Examiner, the claimed
invention is still not provided. The clock line in the SPI Block
Guide is under control of a master device. Reference is directed
to FIG. 4-1 on page 26, for example, where there is no pull-up or
pull-down of the clock SCK line. The clock is entirely under the
control of the master device which uses a Baud Rate Generator to
emit the clock signal. There is no tying of the clock signal from

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a default value to a second value. The slave, too, simply has a shift register to count the clock pulses, and thereby to synchronize itself to the clock signal.

This is also confirmed on page 23, section 4.1, lines 11-12 in the SPI Block Guide, which provides: "When a data transfer operation is performed, this 16-bits register is serially shifted eight positions by the S-clock from the master, so data is exchanged between the master and the slave." (Emphasis added). Reference is also directed to page 24, section 4.3 titled "Slave Mode," lines 1-3, which provides: "The SPI operates in slave mode when the MSTR bit in SPI Control Regsiter1 is clear. - SCK Clock. In slave mode, SCK is the SPI clock input from the master." (Emphasis added).

In other words, characterization of the SPI Block Guide by the Examiner is incorrect. The SPI Block Guide fails to teach or suggest the following that are in the claimed invention:

A) The clock line is not maintained by default on a first logic value;

B) Each device is not provided with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value;

C) The two devices do not tie the clock line to the second logic value after data is applied to the data line;

D) The tying of the clock line is not maintained by the device to which the data is sent while the device has not read the data; and

E) The data on the data line is not maintained by the device sending the data at least until an instant when the clock

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line is released by the device to which the data is sent.

In addition, the Examiner referenced FIG. 4-2 on page 27 in the SPI Block Guide. The Applicants submit this figure is not relevant. In FIG. 4-2, the clock line SCK alternates between the high and the low state (when CPOL=1) but does not teach or suggest how the clock signal SCK is controlled by the devices exchanging data.

Referring now to the SMBus Specification, it appears that open drain lines are used with pull-up polarization (first logic value by default) and pull-down control for sending data having the "second logic value opposite the first logic value". As to the open drain line configuration of the SMBDAT line (data line) and SMBCLK line (clock line), see for example page 9, FIG. 2-1, and page 10, FIGS. 2-2, 2-3 plus the corresponding descriptions associated with these figures.

In other words, the SMBus Specification fails to teach or suggest tying the clock line to the second logic value, via the two devices, after data is applied to the data line. Referring to page 9, lines 2-3, which provides "Generally, a bus master device initiates a bus transfer between it and a single bus slave and provides the clock signals." (Emphasis added). Reference is also directed to page 20, section 4.3.1 titled Synchronization, lines 5-6, which provides: "A high-to-low transition on the SMBCLK line will cause all devices involved to start counting off their LOW period and start driving SMBCLK low if the device is a master".

The SMBus Specification fails to teach or suggest that both the master and the slave device can tie the clock line to a

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second logic value opposite the first logic value. Instead, only
the master device can tie the clock line to a different
potential.

      Moreover, the SMBus Specification fails to teach or
suggest that the tie to the clock line by the device to which the
data is sent is maintained while the device has not read the
data. Even though the SMBus Specification discloses that a slave
device may stretch the clock period, the slave must comply with a
certain timeout.

      Referring to page 12, note 5, which provides: "It is
possible that a slave device or another master will also extend
the clock causing the combined clock low time to be greater than
TLOW-MEXT" (i.e., Cumulative Clock Low Extended Time allowed to
the Master device, see TABLE on page 12). Reference is also
directed to page 13 section 3.1.1.3 titled "Slave device timeout
definition and conditions," which provides: "It is highly
recommended that a slave device release the bus when it detects a
single clock held low longer than Ttimeout, min".

      Reference is also directed to page 22, section 4.3.3
(which the Examiner also references), lines 2-3, which provides:
"In addition to the bus arbitration procedure the clock
synchronization mechanism <u>can be used</u> during a bit or a byte
transfer <u>in order to allow a slower slave device to cope with</u>
<u>faster masters</u>". As illustrated in FIG. 4-7 on page 22, Clock
LOW extension, or stretching, <u>if necessary</u>, must start after the
SMBCLK high-to-low transition. A slave device <u>may opt to stretch</u>
<u>the clock</u> line during a specific bit transfer <u>in order to process</u>
<u>a real time task or check the validity of a byte. In this case</u>

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the slave must adhere to the timeout specifications. A slave device may select to stretch the clock LOW period between byte transfers on the bus in order to process received data or prepare data for transmission.

The SMBus Specification provides a data transfer method on open drain lines which is very different from the claimed invention. In the SMBus Specification, data is stable and is read when the clock signal has a default value (e.g., HIGH since the SMBus Specification provides only a pull-up polarization of the lines), and data is changed when the clock signal is tied to an opposite value (e.g., LOW).

In sharp contrast, the present invention provides a double control of the line by which each device – a master or a slave – can be considered as a master as far as the duration of the clock period is concerned. This advantageously allows each device to impose its operating speed on the other, particularly in the event of disparity of clock frequencies or when one of the devices operates in multitasking on applications that have priority over the data transmission itself.

Accordingly, it is submitted that independent Claim 20 is patentable over the SPI Block Guide in view of the SMBus Specification. Independent Claims 32 and 48 are similar to independent Claim 20. It is submitted that independent Claims 32 and 48 are also patentable over the SPI Block Guide in view of the SMBus Specification.

Independent Claims 44, 46 and 51 are similar to independent Claim 20. It is submitted that independent Claims 44 and 46 are patentable over the SPI Block Guide, and independent

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Claim 51 is patentable over the SMBus Specification.

In view of the patentability of independent Claims 20, 32, 44, 46, 48 and 51, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III.   CONCLUSIONS

In view of the amendments and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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